IN THE SPECIFICATION

Please replace the paragraph at page 13, lines 1-18, with the following rewritten paragraph:

With the semiconductor memory according to the first embodiment, a plurality of inter-electrode dielectrics 8 are arranged on a top surface of the first conductive layers 3, respectively, and are isolated from each other by the device isolation films 7. The inter-electrode dielectrics 8 implement part of the memory transistors belonging to mutually adjacent memory cell columns, respectively. In addition, as shown in Fig. 2, a second conductive layer 10 is arranged upon the inter-electrode dielectrics 8 of respective memory cell columns, and the bottom surface of that second conductive layer makes contact with the top surface of the device isolation films 7. The second conductive layer 10 is formed continuously so as to become a common interconnect to adjacent memory cell columns. As understood by Fig. 3B, actually, a plurality of the second conductive layers 10 run along the row-direction so as to become a plurality of common interconnects to adjacent memory cell columns. The shape of the each of the second conductive layer [[7]] 10 is cut into a ridge shape.